Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1. (original): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming an insulating layer on the semiconductor substrate, including the gate pattern;

anisotropically etching the insulating layer to form sidewall spacers on both sidewalls of the gate pattern and to leave a portion of the insulating layer on the semiconductor substrate, wherein the gate pattern and the sidewall spacers constitute a gate structure;

injecting high concentration impurity ions of the second conductivity type into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing said portion of the insulating layer to expose an upper surface of the heavily doped region, wherein the lightly and heavily doped regions constitute a source/drain;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions.

2. (original): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming sidewall spacers on both sidewalls of the gate pattern to form a gate structure consisting of the gate pattern and the spacers;

forming a buffering layer over the semiconductor substrate, including over the gate structure and the lightly doped regions;

with the buffering layer disposed over the lightly doped regions at both sides of the gate structure, injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing the buffering layer to expose an upper surface of the heavily doped regions and the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

once the buffering layer has been removed, forming a transition metal layer over the semiconductor substrate, including over the sidewall spacers and polysilicon gate of the exposed gate structure and the exposed heavily doped regions; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions;

wherein said buffering layer has a thickness sufficient to prevent the lightly doped regions from becoming damaged during said ion injection for forming said heavily doped regions.

3. (original): The method according to claim 2, wherein said transition metal layer is magnetic.

4. (original): The method according to claim 3, wherein said magnetic transition metal layer comprises at least one selected from a group consisting of cobalt, titanium, or nickel.

5. (original): The method according to claim 2, wherein said buffering layer comprises an insulator.

6. (original): The method according to claim 5, wherein said insulator comprises SiO.sub.2 or SiN.

7. (original): The method according to claim 2, wherein said thickness of said buffering layer is about 30Å..

8. (original): The method according to claim 2, wherein said transition metal layer is formed by physical vapor deposition or chemical vapor deposition using plasma.

9. (currently amended): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

depositing a buffering layer over the semiconductor substrate, including the gate pattern and the lightly doped regions, wherein the thickness of buffering layer is about 30Å or more;

forming sidewall spacers on a portion of the buffering layer at both sidewalls of the gate pattern to produce a gate structure;

injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

removing an exposed portion of the buffering layer to expose upper surfaces of the heavily doped regions and the polysilicon gate;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped region.

10. (previously presented): The method according to claim 9, wherein the buffering layer is a SiO_2 layer.

11. (previously presented): The method according to claim 9, wherein the buffering layer is a SiN layer.

12. (cancelled)

13. (previously presented): The method according to claim 9, wherein the transition metal is made of at least one selected from a group consisting group of Co, Ti, Ni.

14. (currently amended): A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

depositing a buffering layer over the semiconductor substrate, including the gate pattern and the lightly doped regions, wherein the thickness of buffering layer is about 30Å or more;

forming sidewall spacers on a portion of the buffering layer at both sidewalls of the gate pattern to produce a gate structure;

injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

removing an exposed portion of the buffering layer to expose upper surfaces of the heavily doped regions and the polysilicon gate.

15. (previously presented): The method according to claim 14, wherein the buffering layer is a SiO_2 layer.

16. (previously presented): The method according to claim 14, wherein the buffering layer is a SiN layer.

17. (cancelled)